REMARKS

Claims 1-3 and 5-25 are pending in this application, of which claims 7, 14 and 21 are withdrawn from consideration. Reconsideration of the rejections in view of the following remarks is respectfully requested.

Allowable Claims

Applicant gratefully acknowledges that claims 8-13 and 24 were allowed and claims 22, 23 and 25 were merely objected to as depending from a rejected base claim, but are otherwise allowable.

Rejections under 35 USC §103(a)

Claims 1, 2 and 5 were rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al (U.S. Patent No. 5,633,781).

Claim 3 was rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al, and further in view of Foster et al (U.S. Patent No. 5,567,243).

Claim 6 was rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al, and further in view of Applicant admitted prior art.

Applicant respectfully traverses these rejections.

In Saenger et al, an electrically conductive diffusion barrier 8 is formed by a conventional process such as sputtering, and may be $Ta_{1-x}Si_xN_y$ (with $0<<1$ and $y>0$), TiN, or similar materials (col. 4, lines 4-

8). Saenger et al does not teach or suggest, among other things, the step of "(d) heating the semiconductor substrate in a nitriding atmosphere to nitride the plug from a surface thereof."

For at least this reason, claim 1 patentably distinguishes over Saenger et al.

Foster et al has been cited for disclosing the nitriding process using ammonia and a temperature between 600°C to 850°C. Foster et al, however, discusses chemical vapor deposition process but not a process "to nitride the plug from a surface thereof." Thus, Foster et al does not remedy the deficiencies of Saenger et al.

Applicant's admitted prior art has been cited for showing forming the rare metal layer by sputtering followed by a CVD process using oxygen. Such disclosure does not remedy the deficiencies of Saenger et al and Foster et al.

For at least these reasons, claims 2, 3, 5 and 6, depending from claim 1, also patentably distinguish over Saenger et al for at least the same reason.

Thus, the 35 U.S.C. §103(a) rejections should be withdrawn.

Claims 15-20 were rejected under 35 U.S.C. §103(a) as being obvious over Joo (U.S. Patent No. 6,342,425).

Applicant respectfully traverses these rejections.

Joo discloses using a hard mask in place of a resist mask, in the process shown in Figs. 3C and 4C. In the process of Fig. 3C, the lower electrode 50 is patterned using a hard mask such as SiO_2, TiN or Ti. After the patterning step, a dielectric film 60 of PZT is formed to form a capacitor dielectric film. If the hard

mask is not removed and the dielectric film is formed thereon, the desired performance cannot be obtained. SiO_2 is an insulating material, but is not a ferro-electric material, and does not have a high dielectric constant. If the capacitor dielectric film is formed of a stack of silicon oxide film and a PZT film, the effective ferro-magnetic properties will be degraded by the existence of the silicon oxide film. Thus, it cannot be considered to retain the silicon oxide hard mask layer.

TiN and Ti are conductive materials and would not need consideration. If the TiN or Ti layer is not removed, it will serve as part of the lower electrode. The role of rare metal lower electrode will be lost. The capacitor dielectric film of PZT is formed thereon using oxidizing atmosphere. The oxidizing atmosphere will oxidize the surface of the TiN or Ti layer to produce an insulating titanium oxide layer. The titanium oxide layer will degrade the effective function of the PZT dielectric film, similar to the above-mentioned silicon oxide film. Here again, it cannot be considered to retain the hard mask layer and to form an insulating layer thereon.

In Fig. 4C, the stack of the lower electrode 500, the dielectric layer 600, and the upper electrode 700 is patterned. Reference to the hard mask is almost the same as that in Fig. 3C. Thus, it should be understood that the hard mask is removed.

Therefore, Joo does not teach or suggest, among other things, "(f) **forming an insulating film over the semiconductor substrate, the insulating film covering the patterned insulating mask layer**." as recited in claim 15.

For at least these reasons, claims 15 patentably distinguish over Joo. Claims 16-20 depending from claim 15, also patentably distinguish over Joo for at least the same reasons.

Thus, the 35 U.S.C. §103(a) rejections should be withdrawn.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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